

Docket No.: 341148019US00

(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Wright et al.

Application No.: 10/750,456

Confirmation No.: 4971

Filed: December 31, 2003

Art Unit: 3768

For: METHOD AND SYSTEM FOR
CALIBRATION OF A MARKER
LOCALIZATION SENSING ARRAY

Examiner: Ellsworth Weatherby

AMENDED DECLARATION OF J. NELSON WRIGHT UNDER 37 C.F.R. § 1.131

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

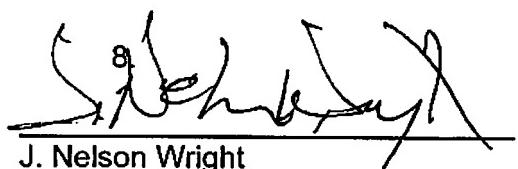
Sir:

I, J. Nelson Wright, declare and state that:

1. I am a joint inventor, along with Lawrence J. Newell of the invention described and claimed in U.S. Patent Application No. 10/750,456 (the "Present Application"), filed on December 31, 2003.
2. This Declaration establishes invention in this country of the subject matter in the currently pending claims in the Present Application before the earliest priority date of U.S. Patent No. 7,158,754 filed on July 1, 2003 by Anderson ("Anderson").
3. All of the work described within this Declaration was performed in the United States, by me or on my behalf and under my direction.
4. I have reviewed my invention disclosure records, including the Exhibit submitted herewith, and readily conclude that the methods and systems as claimed in the Present Application were conceived and reduced to practice

prior to July 1, 2003, the filing date of the Anderson Patent.

5. In support of this conclusion, I have attached Exhibit A, which represents a redacted invention disclosure document entitled "Array Calibration" ("Invention Disclosure"). Although the dates have been removed from the enclosed Invention Disclosure, I represent that this document represents conception of the invention at least prior to July 1, 2003. In particular, a comparison between the figures of the Present Application and the figures of the Invention Disclosure illustrate that the figures in the Invention Disclosure correspond closely to Figures 4-9 of the Present Application.
6. Further in support of this conclusion, I have attached Exhibit B, which represents a redacted schematic drawing of a working prototype of the array disclosed and claimed in the pending US Application 10/750,456 dated at least prior to July 1, 2003. This schematic drawing is evidence of actual reduction to practice prior to the July 1, 2003 critical date of Anderson.
7. I further declare that all statements herein made of my own knowledge are true and that all statements made on information or belief are believed to be true; and further, that the statements are made with the knowledge that the making of willful or false statements or the like is punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and may jeopardize the validity of any patent issuing from the present patent application.



J. Nelson Wright

10 September 2009

Date

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Enclosure:

Exhibit A

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EXHIBIT A

Array Calibration

Objective:

The objectives of this writeup are to:

- 1) Reformulate Nelson's writeup of calibration from 11/19/02 in terms of differential and common-mode calibration operations. The primary motivation for doing this is to reduce the number of calibration operations which must be executed dynamically (up to a four-fold reduction).
- 2) Extend Nelson's writeup to include treatment of additional pertinent parasitic elements or error sources to be incorporated for accurate calibration.
- 3) Specify the calibration algorithm and EEPROM contents in sufficient detail to allow software developers to code the algorithm.

Outline:

The outline of this description is follows:

- 1) Calibration Architecture
- 2) Single-ended vs. Differential-Mode/Common-Mode Representation
- 3) Model of Array Admittances
- 4) Dynamic vs. Static Calibration
- 5) Mitigation of channel-channel mismatch in voltage calibration sources
- 6) Effects of Differential Imbalance in the voltage calibration sources
- 7) Effect of feedthrough and crosstalk in the Calibration Drive Circuitry
- 8) Parameters to be stored in EEPROM.
- 9) Summary of the calibration algorithm.

1) Calibration Architecture:

Figure 1a is a schematic of a single differential preamplifier and associated calibration sources for the Pharos sense array. The preamplifier and array are discussed in detail elsewhere. The precision calibration sources are implemented by switching square-wave waveforms into any of four injection ports per differential preamplifier channel. The two injection ports through large-valued, precision resistors R_{ref} make up the I_{CAL} , or current injection calibration ports. The two injection ports through precision resistor dividers (R_{DIV1} and R_{DIV2}) constitute the V_{CAL} , or voltage calibration ports. The square-wave waveforms are generated with registers implemented in the AC family of CMOS logic. This family of logic switches the register outputs to either GND or V_s through very low-valued switch resistances. A stable and accurate supply voltage V_s guarantees that square-waves of precise amplitude and phase are generated. The calibration sources can be activated in any desired pattern, either singly, differentially, or in common-mode. The receiver board contains filtering to eliminate all higher harmonics leaving only the fundamental of the calibration waveform. All signal-path circuitry is operated in a highly linear manner.

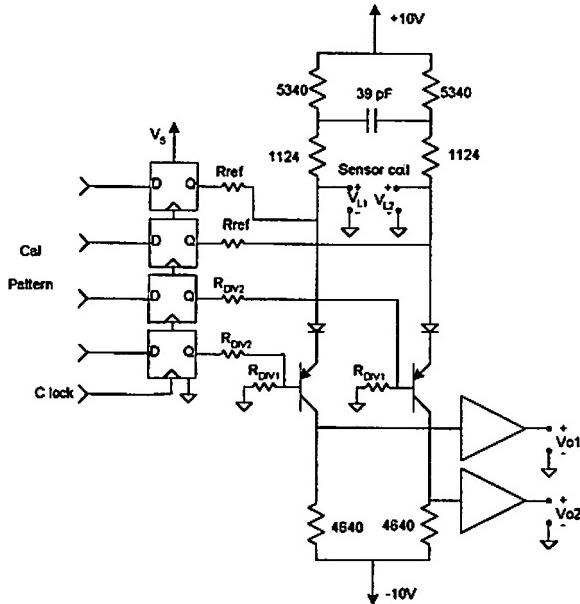


Figure 1a

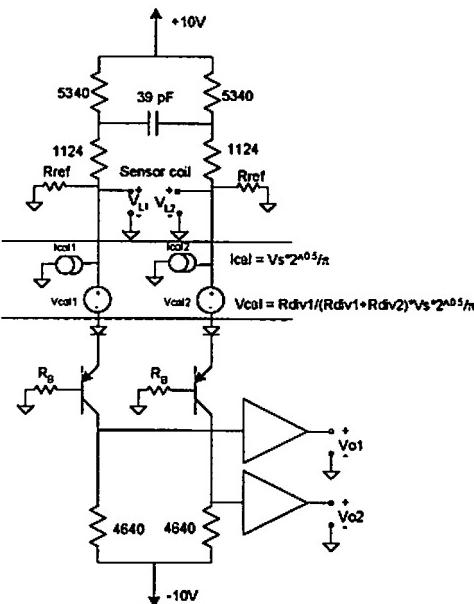
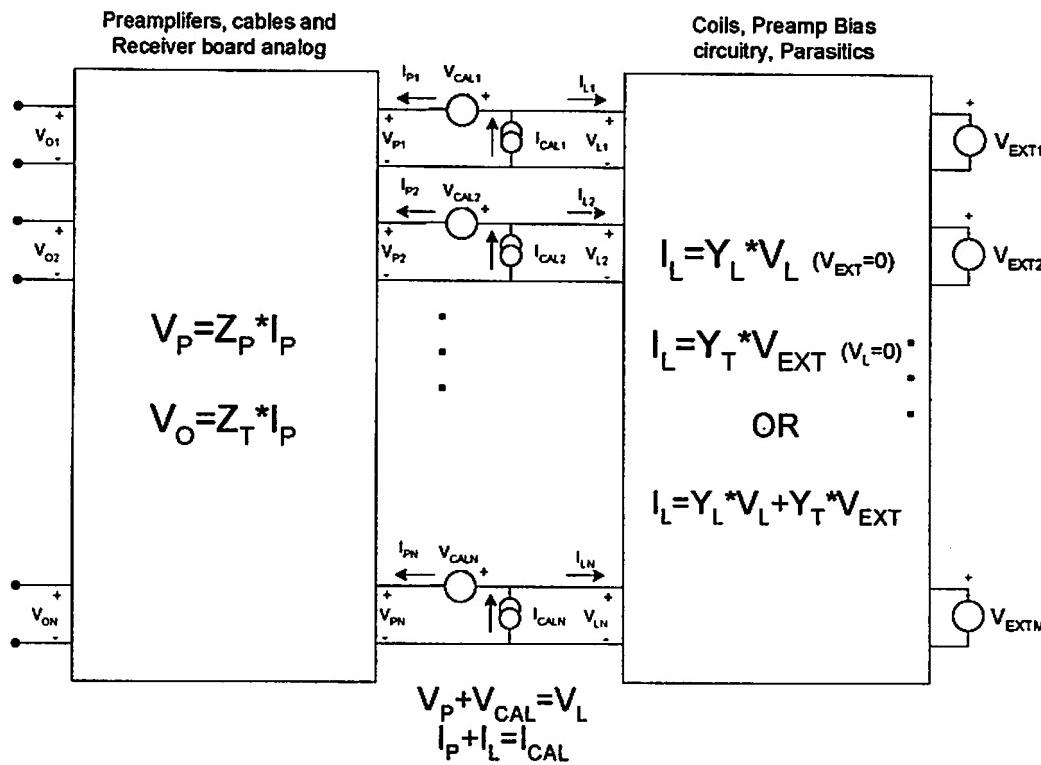


Figure 1b

Figure 1b is an equivalent circuit of the single differential preamplifier from figure 1a which can be derived using the hybrid-pi model assuming no impedance between the collector and base terminals of the transistor. The square-wave calibration sources have been replaced by idealized sinusoidal voltage and current sources with rms amplitudes related to the supply voltage V_s as shown in the figure.

Figure 2, depicts the entire $M=32$ coil array, $N=64$ current calibration sources, N voltage calibration sources and the network consisting of $N/2=32$ differential preamplifiers. As indicated by the dashed lines in figure 1b, for analysis purposes, the R_{ref} resistor, snubber and biasing network are incorporated in the Y_L array matrix. The V_{EXT} vector represents the induced open-circuit Faraday voltage in the M sense coils. The $N \times M$ Y_T ‘transadmittance’ matrix relates the N short-circuit currents I_L measured at the calibration current injection points to the M elements of V_{EXT} . $N \times N$ Y_L represents the ‘self-admittance’ of the array as measured from the calibration current injection points. Note that the $N=2 \times M$ 2-ports on the left of the array can be considered as single-ended signals referred to a common reference, or as M differential ports and M common-mode ports referred to a common reference (with consistent representations of Y_L and Y_T).



Similarly, the preamps, cables and receiver board are characterized by an NxN (64x64) complex ‘transimpedance’ Z_T matrix, an NxN complex ‘self-impedance’ Z_P matrix, Nx1 output voltage vector V_O , Nx1 input voltage vector V_P and Nx1 input current I_P .

The N calibration current sources I_{CAL} and N calibration voltage sources V_{CAL} are related to the array and preamp voltages and currents by the nodal equations shown in the figure.

In normal (localization) operation, $V_{CAL}=0$ and $I_{CAL}=0$ and the output voltage vector V_O and the ‘hypothetical’ short-circuit current I_{L_SC} can be found using the equations in the figure from the V_{EXT} voltages:

$$\begin{aligned} V_O &= -Z_T \cdot (I_{MxM} + Y_L \cdot Z_P)^{-1} \cdot Y_T \cdot V_{EXT} \\ &= -T^{-1} \cdot Y_T \cdot V_{EXT} \\ I_{L_SC} &= Y_T \cdot V_{EXT} \\ &= -T \cdot V_O \end{aligned}$$

Thus multiplying the measured output voltage vector by T gives the short-circuit current measurement of the array. T^{-1} is defined as follows and is measured during calibration:

$$T^{-1} = Z_T \cdot (I_{MxM} + Y_L \cdot Z_P)^{-1}$$

During excitation of the calibration currents, with $V_{CAL}=0$ and $V_{EXT}=0$:

$$V_O = Z_T \cdot (I_{MxM} + Y_L \cdot Z_P)^{-1} \cdot I_{CAL}$$

$$= T^{-1} \cdot I_{CAL}$$

During excitation of the calibration voltage, with $I_{CAL}=0$ and $V_{EXT}=0$:

$$V_O = -Z_T \cdot (I_{MxM} + Y_L \cdot Z_P)^{-1} \cdot Y_L \cdot V_{CAL}$$

$$= -T^{-1} \cdot Y_L \cdot V_{CAL}$$

A calibration sequence consisting of measuring column vector V_O while stepping through each of the I_{CAL} elements one at a time measures the columns of T^{-1} . Stepping through each of the V_{CAL} elements one at a time measures the columns of $T^{-1} \cdot Y_L$. This architecture then allows us to measure Y_L , and to measure the short-circuit current resulting from V_{EXT} : $I_{L_SC} = Y_T \cdot V_{EXT}$. All we have to do now is relate the measured NxN Y_L to the needed NxM Y_T , and we can determine, with high accuracy, the original V_{EXT} .

2) Single-ended representation vs. Differential-Mode/Common-Mode representation:

As we have a fully differential circuit topology throughout the array and receive signal chain, there are advantages to representing the Z, Y and T matrices noted above with M=32 differential and M=32 common mode ports, rather than N=2M=64 single-ended ports. Each port always consists of two terminals. The single-ended and common-mode ports always use the common ground reference as one terminal, the differential ports do not use a ground reference.

Denoting I_+ , I_- , V_+ and V_- as 32×1 column vectors corresponding to the positive and negative single-ended terminal currents and voltages for the 32 pairs of ports of our Y matrix, we can create the 64×1 column vectors and 64×64 Y matrix segmented as follows:

$$\begin{bmatrix} I_+ \\ I_- \end{bmatrix} = \begin{bmatrix} Y_{++} & | & Y_{+-} \\ \hline Y_{-+} & | & Y_{--} \end{bmatrix} \begin{bmatrix} V_+ \\ V_- \end{bmatrix}$$

Alternately, we may perform the coordinate transformation to differential and common-mode currents and voltages:

$$I_D = (I_+ - I_-)/2$$

$$I_C = (I_+ + I_-)/2$$

$$V_D = V_+ - V_-$$

$$V_C = V_+ + V_-$$

$$\left[\begin{array}{c} I_D \\ I_C \end{array} \right] = \left[\begin{array}{c|c} Y_{DD} & Y_{DC} \\ \hline Y_{CD} & Y_{CC} \end{array} \right] \left[\begin{array}{c} V_D \\ V_C \end{array} \right] = \frac{1}{4} \left[\begin{array}{c|c} Y_{++} + Y_{--} - Y_{+-} - Y_{-+} & Y_{++} - Y_{--} + Y_{+-} - Y_{-+} \\ \hline Y_{++} - Y_{--} + Y_{+-} - Y_{-+} & Y_{++} + Y_{--} + Y_{+-} + Y_{-+} \end{array} \right] \left[\begin{array}{c} V_D \\ V_C \end{array} \right]$$

Y_{DD} represents the short-circuit differential current for a differential voltage drive.

Y_{CC} represents the short-circuit common-mode current for a common-mode voltage drive.
 Y_{DC} and Y_{CD} represent the mode coupling admittances.

3) Model of Array Admittances:

This section will discuss the relation of the measurable Y_L (admittance measured from the array coil terminals) to the desired Y_T (the transadmittance from the Faraday induced voltage to the array coil terminals).

A number of different intentional circuit elements and unintentional (parasitic) circuit elements contribute to the total Y_L . It can be shown that the admittances from these other elements just add to the desired transadmittance, Y_T . Determining Y_T from the measured Y_L just involves determining and subtracting off the undesired components of Y_L .

Three types of array admittances can be identified with respect to calculating the desired Y_T .

$$Y_L = Y_{L1} + Y_{L2} + Y_{L3}$$

- 3.1) The ‘ideal’ sense coils themselves: These components have no common mode admittance and no common to differential or differential to common mode coupling terms. The differential admittance is just the M_c^{-1} matrix described in Nelson’s writeup. Note that the 64x32 Y_T is just the first 32 columns of Y_{L1} .

$$Y_{L1} = \left[\begin{array}{c|c} Y_{L1DD} & Y_{L1DC} \\ \hline Y_{L1CD} & Y_{L1CC} \end{array} \right] = \left[\begin{array}{c|c} M_c^{-1} & 0 \\ \hline 0 & 0 \end{array} \right]$$

$$Y_T = \left[\begin{array}{c} Y_{TDD} \\ \hline Y_{TCD} \end{array} \right] = \left[\begin{array}{c} M_c^{-1} \\ \hline 0 \end{array} \right]$$

- 3.2) Circuit elements which are connected directly between array coil terminals and the common reference ground potential: These components have a differential-mode admittance that is equal to the common-mode admittance. The differential mode components can be determined by measurement of the common-mode components of Y_L . Examples in this category include:
- Preamp bias resistors
 - Impedance of the Norton equivalent resistor for the current cal. source Rref
 - Stray capacitance to GND of differential pairs and coil
- All these components show up only on the diagonal of each block. In general, these components are reasonably well matched (~1%) and fairly small to start

with. If the shunt impedances to GND are denoted $z_{1p}, z_{1n}, z_{2p}, z_{2n}, \dots, z_{Np}, z_{Nn}$, then the admittance matrix looks like:

$$Y_{L2} = \begin{bmatrix} Y_{DD} & | & Y_{DC} \\ \hline Y_{CD} & | & Y_{CC} \end{bmatrix} = \frac{1}{4} \begin{bmatrix} z_{1p}^{-1} + z_{1n}^{-1} & 0 & \cdots & 0 & | & z_{1p}^{-1} - z_{1n}^{-1} & 0 & \cdots & 0 \\ 0 & z_{2p}^{-1} + z_{2n}^{-1} & \cdots & 0 & | & 0 & z_{2p}^{-1} - z_{2n}^{-1} & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots & | & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & z_{Np}^{-1} + z_{Nn}^{-1} & | & 0 & 0 & \cdots & z_{Np}^{-1} - z_{Nn}^{-1} \\ \hline z_{1p}^{-1} - z_{1n}^{-1} & 0 & \cdots & 0 & | & z_{1p}^{-1} + z_{1n}^{-1} & 0 & \cdots & 0 \\ 0 & z_{2p}^{-1} - z_{2n}^{-1} & \cdots & 0 & | & 0 & z_{2p}^{-1} + z_{2n}^{-1} & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots & | & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & z_{Np}^{-1} - z_{Nn}^{-1} & | & 0 & 0 & \cdots & z_{Np}^{-1} + z_{Nn}^{-1} \end{bmatrix}$$

- 3.3) Those elements whose common-mode and differential-mode admittances are not the same, and hence must be characterized in engineering or in the factory and included in the EEPROM. There are two types here, which will be modeled separately.

$$Y_{L3} = Y_{L3A} + Y_{L3B}$$

The first type, Y_{L3A} covers the differential shunt impedance across each coil. This is from the intentional snubber network, and the unintentional parasitic capacitance across the coil and differential pairs leading from the coil. If these individual impedances are denoted $z_{31}, z_{32}, \dots, z_{3N}$, the admittance matrix looks like:

$$Y_{L3A} = \begin{bmatrix} Y_{DD} & | & Y_{DC} \\ \hline Y_{CD} & | & Y_{CC} \end{bmatrix} = \begin{bmatrix} z_{31}^{-1} & 0 & \cdots & 0 & | & 0 & 0 & \cdots & 0 \\ 0 & z_{32}^{-1} & \cdots & 0 & | & 0 & 0 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots & | & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & z_{3N}^{-1} & | & 0 & 0 & \cdots & 0 \\ \hline 0 & 0 & \cdots & 0 & | & 0 & 0 & \cdots & 0 \\ 0 & 0 & \cdots & 0 & | & 0 & 0 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots & | & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & 0 & | & 0 & 0 & \cdots & 0 \end{bmatrix}$$

The second type, Y_{L3B} , covers the small capacitive coupling between the differential pairs and coils in the array. Unfortunately, this is not expected to appear mainly common-mode or differential mode. However it will have 0's on the diagonals of each block. This type will need to be characterized in differential mode and stored in EEPROM.

Thus to determine the desired $Y_{TDD} = M_C^{-1}$ we take the measured differential Y_{LDD} , subtract the Y_{L3ADD} and Y_{L3BDD} derived from the EEPROM contents, and subtract the diagonal elements of the measured common-mode $Y_{LCC\text{diagonal}}$,

$$Y_{TDD} = M_C^{-1} = Y_{L_{DD}} - Y_{L_{3A_{DD}}} - Y_{L_{3B_{DD}}} - Y_{L_{CC\text{diagonal}}}$$

Note that only the diagonal elements of the measured Y_{LCC} should be subtracted off. The off-diagonal elements include common-mode capacitance (Y_{L3BCC}) between the coils that do not affect Y_T .

4) Dynamic vs. Static Calibration:

Some of the array and receiver parameters discussed above are subject to variation with temperature (such as the preamp gain and input impedance represented by Z_T , Z_P and T). Other parameters such as Y_T , Y_L or M_C are subject to variation on much shorter time scales as metal objects may be introduced to or removed from the vicinity of the array. Still others are expected to remain essentially static over time, such as Y_{LCC} . It is therefore important to execute measurements of the time-varying parameters interleaved with localization measurements to assure accurate calibration of the Pharos system.

Executing calibration measurements frequently, however, reduces the percentage of time during which localization measurements can be made, which in turn will impact adversely either the update rate or variance of the localization measurements.

As only one block of the Y_L matrix, Y_{LDD} , is prone to variation, we can save considerable time by exciting the VCAL sources in differential mode only, and making only the differential receive measurement. This reduces by 75% the time required to make the voltage calibration measurements.

A similar 75% savings can be achieved in the current calibration measurements if the T matrix is block-diagonal. In the calibration process outlined in section 1, the columns of T^{-1} are measured sequentially, and the desired T matrix is calculated with a matrix inversion. In general, the full T^{-1} matrix must be measured to determine T , but if T^{-1} is block-diagonal, the diagonal blocks can be measured and inverted independently.

$$\begin{bmatrix} Tinv_{DD} & 0 \\ 0 & Tinv_{cc} \end{bmatrix}^{-1} = \begin{bmatrix} Tinv_{DD}^{-1} & 0 \\ 0 & Tinv_{cc}^{-1} \end{bmatrix}$$

In the Pharos system, measurements of the T^{-1} matrix indicate that the off-diagonal blocks are 40 to 50 dB smaller than the diagonal blocks. The error introduced in making the block-diagonal assumption in the matrix inversion goes as the square of the relative magnitudes of the off-diagonal blocks. We can then expect errors of less than 100 ppm in making this assumption.

Thus only differential-mode excitation and differential-mode receive measurements need to be made dynamically. The full calibration need only be executed on a much less frequent basis, such as once per patient, once per day, or even just once in the factory.

5) Mitigation of channel-to-channel mismatch in voltage calibration sources:

In characterizing Y_L one column at a time, the ‘short-circuit’ current is measured while driving one channel (differentially, or common-mode) at a time. Mismatches in the individual (single-ended) calibration voltage sources result in the following effects:

- Channel-channel amplitude mismatch in the differential drive voltages
- Channel-channel amplitude mismatch in the common-mode drive voltages.
- Crosstalk into the common mode when driving differentially
- Crosstalk into the differential mode when driving common-mode.

Crosstalk between modes is treated in the next section.

Mismatches in the current calibration sources are expected to be limited by the accuracy of the R_{REF} resistor, or about 0.02%. Achieving this type of accuracy in the VCAL voltage dividers, though, is not feasible.

Mismatches in the voltage divider unique to each channel will result in gain errors common to each column of the measured admittance. Let Y_M be the measured (corrupted) admittance, and G_V^{-1} be the (complex) diagonal matrix representing the (unknown) gain errors that caused the corruption:

$$Y_M = Y_L \cdot G_V^{-1}$$

$$Y_L = Y_M \cdot G_V$$

We want to find that $G_V = \text{diag}\{[g_1 \ g_2 \ g_3 \ \dots \ g_{32}]\}$ to correct the measured Y_M and achieve the true Y_L . Reciprocity will guarantee that Y_L is a symmetric matrix. A least squares fit can be applied to ‘back out’ the differential voltage drive mismatches that were present. The equations describing reciprocity of Y_L are:

$$\begin{array}{ll} Y_{L12} = Y_{L21} & Y_{M12}g_2 = Y_{M21}g_1 \\ Y_{L13} = Y_{L31} & Y_{M13}g_3 = Y_{M31}g_1 \\ \vdots & \vdots \end{array} \quad \text{or} \quad \begin{array}{l} \\ \\ \end{array}$$

This is a system of $\frac{1}{2}*(32^2-32)=496$ equations with only 32 (complex) unknowns ($g_1 \dots g_{32}$). Of course the least squares fit to this system of equations will be $g_1=g_2=\dots=g_{32}=0$. To assure the solution we want, we need to add one more equation that assures the mean of the gains is 1: $g_1+g_2+\dots+g_{32}=32$.

This system of equations can be captured in matrix form as:

$$A \cdot g = b$$

with:

$$g = [g_1 \ g_2 \ g_3 \ \cdots \ g_{31} \ g_{32}]^T$$

$$b = [0 \ 0 \ 0 \ 0 \ 0 \ \cdots \ 0 \ 0 \mid 32]^T$$

$$A = \left[\begin{array}{cccccc} y_{M21} & -y_{M12} & 0 & \cdots & 0 & 0 \\ y_{M31} & 0 & -y_{M13} & \cdots & 0 & 0 \\ 0 & y_{M32} & -y_{M23} & \cdots & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ 0 & 0 & 0 & \cdots & y_{M3231} & -y_{M3132} \\ \hline 1 & 1 & 1 & \cdots & 1 & 1 \end{array} \right]$$

The least squares solution to this overdetermined system of equations is:

$$g = (A^H A)^{-1} A^H b$$

$$G_\nu = \text{diag}\{g\}$$

Any differential-mode channel-channel mismatch should also be present in the common-mode measurement. The same voltage source error fit obtained to achieve a symmetrical Y_L in the differential block should be applied to the common-mode block as well.

6) Effects of Differential Imbalance in the calibration drive voltage sources V_{CAL} :

Crosstalk from the differential mode to the common-mode can be analyzed as follows. When driving channel 1 differentially:

$$I_{L_sc} = -T \cdot V_o = Y_L \cdot V_{CAL} = \left[\begin{array}{c|c} Y_{DD} & Y_{DC} \\ \hline Y_{CD} & Y_{CC} \end{array} \right] \cdot \left[\begin{array}{c} V_{CAL_D} \\ \hline V_{CAL_C} \end{array} \right]$$

$$V_{CAL} = [V \ 0 \ \cdots \ 0 \mid \epsilon V \ 0 \ \cdots \ 0]^T$$

instead of measuring just the first column of Y_{DD} , we will also get ϵ times the first column of Y_{DC} added to it.

Y_{DC} contains only the mismatch in Y_{L2} shunt components, and Y_{L3B} stray capacitances. For a rough order of magnitude estimate ... the shunt elements in Y_{L2} have 1/10 the admittance of the diagonal elements of Y_{DD} . The mismatch in these elements (which is what Y_{DC} contains) is probably < 1/30 times that. Finally, ϵ is on the order of 1/1000. This makes this error term on the order of 3 ppm of the diagonal elements of Y_{DD} , and should be negligible.

Crosstalk from common-mode to differential mode will be the same order of magnitude.

7) Effect of Feedthrough and Crosstalk in the Calibration Drive Circuitry:

There are 4 types of feedthrough from calibration drive circuitry to the V_O output to consider:

- Parasitic paths coupling the current-drive waveform into the V_O output – diagonal terms.

The dominant path expected here is the small amount of capacitance across the R_{REF} resistor. Measurements indicate this is below 0.1 pF. At 500 kHz, this results in a gain error below 1 part per 10,000. Also, the layout of each channel is identical, so this gain error should be the same across all channels. This effect will be ignored (but verified in the hardware).

- Parasitic paths coupling the current-drive waveform into the V_O output - off-diagonal terms.

Every attempt was made to minimize the possibility of this. For now, we will assume we don't have to compensate for this effect. This will be verified on the hardware by just removing the R_{REF} resistor and measuring the S-vectors received in current calibration mode.

- Parasitic paths coupling the voltage-drive waveform into the V_O output – diagonal terms.

A significant effect is expected here from the collector-base capacitance in the preamp PNP transistor. We have not yet attempted to incorporate this in the circuit model, but errors from this source should be effectively mitigated by measuring and subtracting off the common-mode array admittance. In measuring the common-mode array admittance, the collector-base capacitance will appear as a 'negative' capacitance to GND in the array. This effect is present to the same degree in both differential and common-mode drive, so subtracting $Y_{LCCDiagonal}$ from the measured Y_{LDD} should be effective in compensating for this.

- Parasitic paths coupling the voltage-drive waveform into the V_O output - off-diagonal terms.

As with the off-diagonal current-drive terms, we're hoping for the best on this one for now.

There is also the potential for crosstalk between current-drive and voltage drive sources or between channels. Again, every attempt has been made to minimize this in the layout, and we will not attempt to treat this at this time.

8) Summary of EEPROM stored data:

EEPROM Stored Data:

- Rref: Current calibration reference impedance
 Single real 16 bit value (in ohms)
 Nominal Value = 49900 (49.9 Kohms)
- Kdiv: Differential Voltage calibration divisor ratio.
 Single real 16 bit value (x1e-6)
 Nominal Value = 6350 (0.006350)
- R₁,R₃: Sense Coil snubber/bias resistance values.
 Two real 16 bit values (in ohms)
 Nominal Values = 1124,5340
- Csnub: Sense Coil snubber resistance value
 Single real 16 bit value (in 0.01 pF)
 Nominal Value = 3900 (39 pF)
- C_{3A}: Parasitic differential shunt capacitance across sense coils
 32 real 16 bit values (in 0.01 pF)
 Nominal Value = 500 (5 pF)
- C_{3B}: Differential mode parasitic capacitance between sense coils
 ~100 non-zero values of upper-triangular 32x32 real matrix of 16 bit
 values (in 0.01 pF) (nearest neighbors only)
 Nominal Value = 500 (5 pF) for nearest neighbors
- Y_{LDD diagonal}: Results of dynamic cal in the factory at 300kHz, 400 kHz, 500 kHz
 32x3 complex 16 bit values (in units of 100 nS)
 Nominal value at 300 kHz = 6835 - j*47240 (6.835e-4 - j*4.724e-3 S)
 Nominal value at 400 kHz = 3879 - j*35751 (3.879e-4 - j*3.575e-3 S)
 Nominal value at 500 kHz = 2493 - j*28721 (2.493e-4 - j*2.872e-3 S)
- Y_{LLC diagonal}: Results of static cal in the factory at 300kHz, 400 kHz, 500 kHz
 32x3 complex 16 bit values (in units of 100 nS)
 Nominal value at 300 kHz = 874 - j*377 (8.74e-5 - j*3.77e-5 S)
 Nominal value at 400 kHz = 874 - j*503 (8.74e-5 - j*5.03e-5 S)
 Nominal value at 500 kHz = 874 - j*628 (8.74e-5 - j*6.28e-5 S)

Calculation of Y_{L3A} and Y_{L3B} from EEPROM Stored Data:

Let s=j*2*pi*Fc where Fc is the operating center frequency (unique for each beacon).

For Y_{L3A}, first we calculate the differential admittance of the snubber/bias network, and subtract off the common mode admittance of the snubber/bias network (which is accounted for in the common-mode measurement). This is a single parameter for all channels.

$$Y_{SNUB} = \frac{1}{2(R_1 + \frac{R_3}{2R_3 C_{SNUB} s + 1})} - \frac{1}{2(R_1 + R_3)}$$

To get Y_{L3A} , we then add the per channel capacitances, C_{3A} .

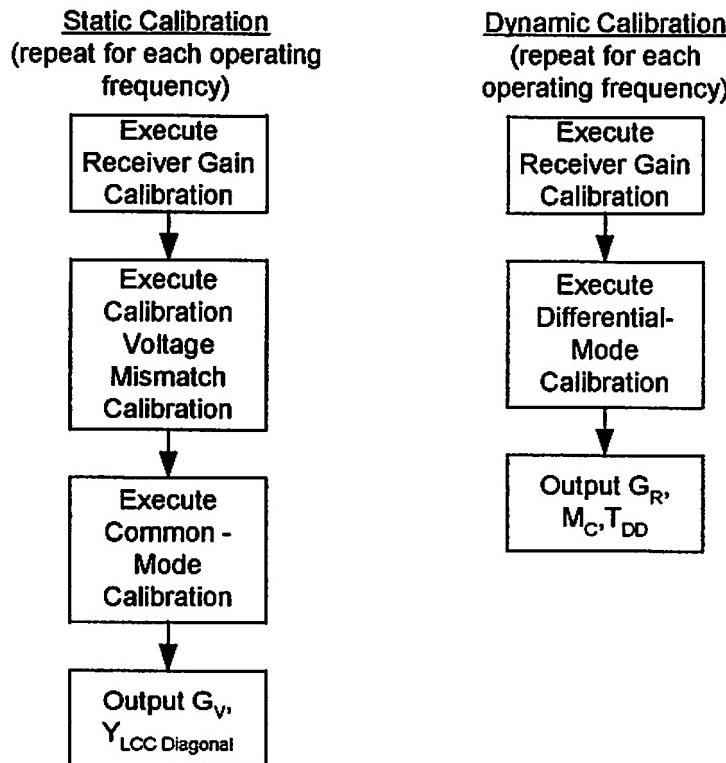
$$Y_{L3A} = Y_{SNUB} \cdot I_{32 \times 32} + \text{diag}\{sC_{3A}\}$$

Y_{L3B} is just s times a capacitance matrix. This matrix is calculated by populating the non-zero elements and adding its transpose. (The pattern of non-zero elements to be updated later).

$$Y_{L3B} = s \cdot (C_{3B} + C_{3B}^T)$$

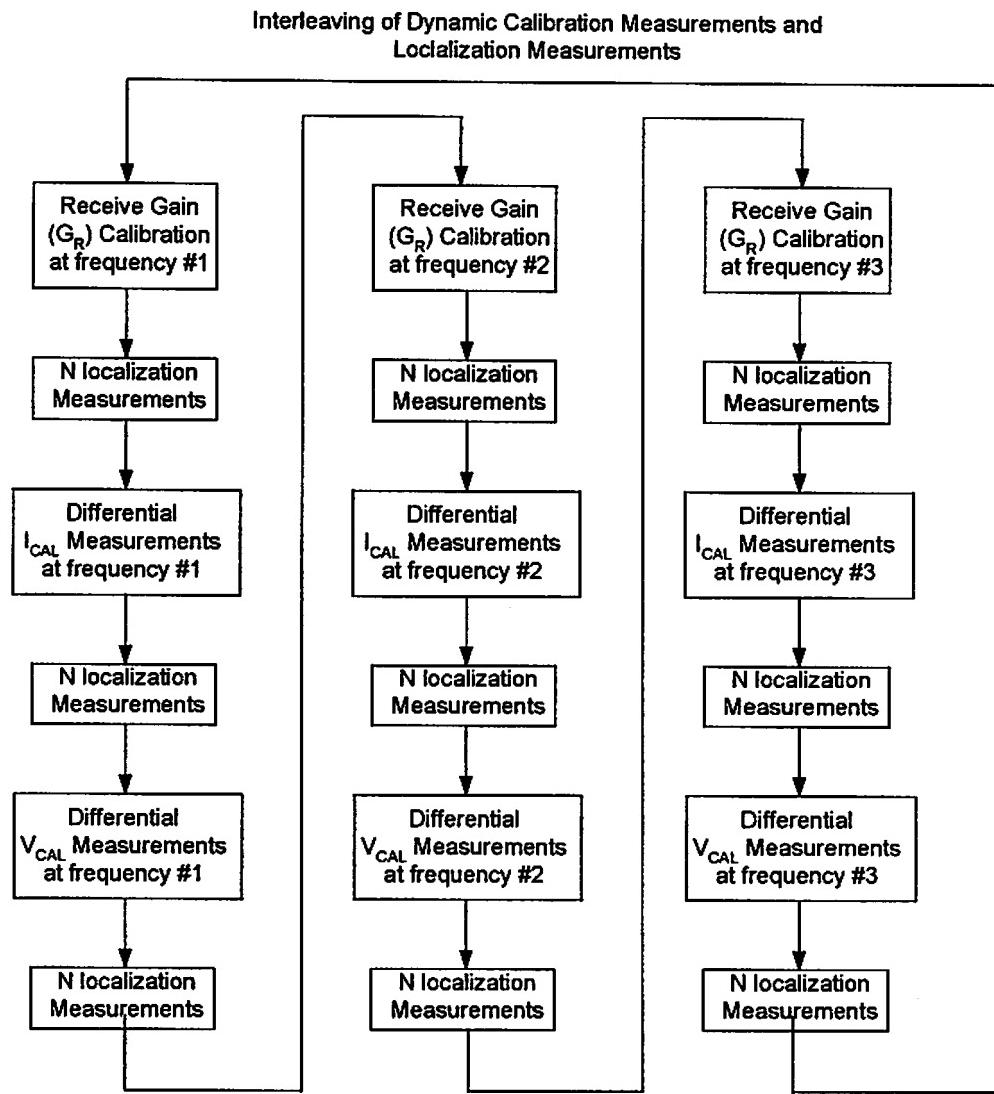
9) Summary of the Calibration Algorithm:

All calibration operations discussed are divided into two software processes: Static Calibration and Dynamic Calibration. Static calibration is currently planned to be executed at 'Session test' at the beginning of treatment for each patient. Dynamic Calibration is interleaved with localization measurements. The figures below indicate the processes involved with each. The individual blocks are described in more detail subsequently.



The next block describes how dynamic calibration measurements are interleaved with localization measurements. Note that N will be typically around 4. Each localization measurement will require roughly 100 msec. Each calibration block will require

roughly 40 msec. Executing the full dynamic calibration cycle will then take roughly 4 seconds.



Receiver Gain (G_R) Calibration

The objective of Receiver Gain Cal is to back out gain errors associated with the higher gain typically used in localization (G_R^{-1}). Calibration is performed at the low-gain setting. If localization is performed with the low-gain setting, no correction is needed. If localization is performed with the high-gain setting, the measured S-vectors should be left-multiplied by G_R prior to any other processing.

The following steps are performed in receive gain cal:

- 1) Configure receiver front-end for high-gain with inputs selected to V_{CM}
- 2) Measure S_{HIGH} complex values with cal-kernel, $NMSI=1$

- 3) Configure receiver front-end for low-gain with inputs selected to V_CM
- 4) Measure S_LOW complex values with cal-kernel, NMSI=1
- 5) Form gr_inv, a 32x1 complex vector by taking the element-by element ratio of S_HIGH over S_LOW.
- 6) Calculate $G_R = (\text{diag}\{\text{gr_inv}\})^{-1}$
- 7) Output G_R

Calibration Voltage Mismatch (G_V) Calibration:

The objective of this process is to determine the channel-channel gain mismatches present in the calibration voltage sources.

The following steps are performed to determine G_V :

1. Configure receiver in low gain and differential reception
2. Excite Cal Current sources one at a time differentially. The 32 sets of measured S vectors form the matrix $S_{ICAL_{DD}}$.
3. Excite Cal Voltage sources one at a time differentially. The 32 sets of measured S vectors form the matrix $S_{VCAL_{DD}}$.
4. Calculate T_{DD} , $Y_{LDD\text{Measured}}$, as follows:

$$T_{DD} = \frac{1}{R_{REF}} (S_{ICAL_{DD}})^{-1}$$

$$Y_{LDD\text{Measured}} = -\frac{1}{K_{DIV}} T_{DD} \cdot S_{VCAL_{DD}}$$

5. Form the matrix A from the elements of $Y_{LDD\text{Measured}}$ and construct the vector b as described in section 4.
6. Obtain the correction gain vector g and matrix G_V as follows:

$$g = (A^H A)^{-1} A^H b$$

$$G_V = \text{diag}\{g\}$$

7. Output G_V .

Common-Mode Calibration:

The objective of this process is to measure the diagonal terms of the common-mode block of Y_L , designated as $Y_{LCC\text{Diagonal}}$.

The following steps are performed to determine $Y_{LCC\text{Diagonal}}$:

- 1) Configure receiver in low gain and single-ended receive (+ terminal)

- 2) Excite Cal Current sources one at a time in common-mode. The 32 sets of measured S vectors form the matrix $S_{ICAL_{C+}}$.
- 3) Repeat steps 1 and 2 for – terminal to collect S_{ICAL_C} .
- 4) Excite Cal Voltage sources one at a time in common mode receiving single-ended both + and – terminals. The two 32x32 sets of measured S vectors form the matrices $S_{VCAL_{C+}}$ and S_{VCAL_C} .
- 5) Calculate T_{CC} and use G_V (see below) to calculate $Y_{LCC\text{Diagonal}}$ as follows:

$$T_{CC} = \frac{1}{R_{REF}} (S_{ICAL_{C+}} - S_{ICAL_C})^T$$

$$Y_{LCC} = -\frac{1}{K_{DIV}} T_{CC} \cdot (S_{VCAL_{C+}} - S_{VCAL_C}) \cdot G_V$$

Zero out all non-diagonal elements of Y_{LCC} to form $Y_{LCC\text{Diagonal}}$

- 6) Output $Y_{LCC\text{Diagonal}}$.

Differential-Mode Calibration

The two objectives of differential-mode calibration are to:

- Frequently update the differential block of the T matrix relating measured S values to short circuit current at the preamp inputs
- Frequently update the transfer function from V_{EXT} to differential short circuit current at the preamp inputs (ie M_C^{-1}).

The following steps are performed for Differential Cal:

1. Configure receiver in low gain and differential reception
2. Excite Cal Current sources one at a time differentially. The 32 sets of measured S vectors form the matrix $S_{ICAL_{DD}}$.
3. Excite Cal Voltage sources one at a time differentially. The 32 sets of measured S vectors form the matrix $S_{VCAL_{DD}}$.
4. Calculate T_{DD} , $Y_{LDD\text{Measured}}$, and M_C as follows:

$$T_{DD} = \frac{1}{R_{REF}} (S_{ICAL_{DD}})^T$$

$$Y_{LDD\text{Measured}} = -\frac{1}{K_{DIV}} T_{DD} \cdot S_{VCAL_{DD}}$$

$$Y_{LDD\text{Corrected}} = Y_{LDD\text{Measured}} \cdot G_V - Y_{LCC\text{Diagonal}} - Y_{L3A} - Y_{L3B}$$

$$M_C = \left(\frac{1}{2} Y_{LDD\text{Corrected}} + \frac{1}{2} Y_{LDD\text{Corrected}}^T \right)^T$$

5. Output T_{DD} and M_C .

Application of Calibration Results to raw S vectors for Localization:

$$S_{CORRECTED} = M_C \cdot T_{DD} \cdot G_R \cdot S_{RAW}$$

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(PATENT)

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In re Patent Application of:
Wright et al.

Application No.: 10/750,456

Confirmation No.: 4971

Filed: December 31, 2003

Art Unit: 3768

For: METHOD AND SYSTEM FOR
CALIBRATION OF A MARKER
LOCALIZATION SENSING ARRAY

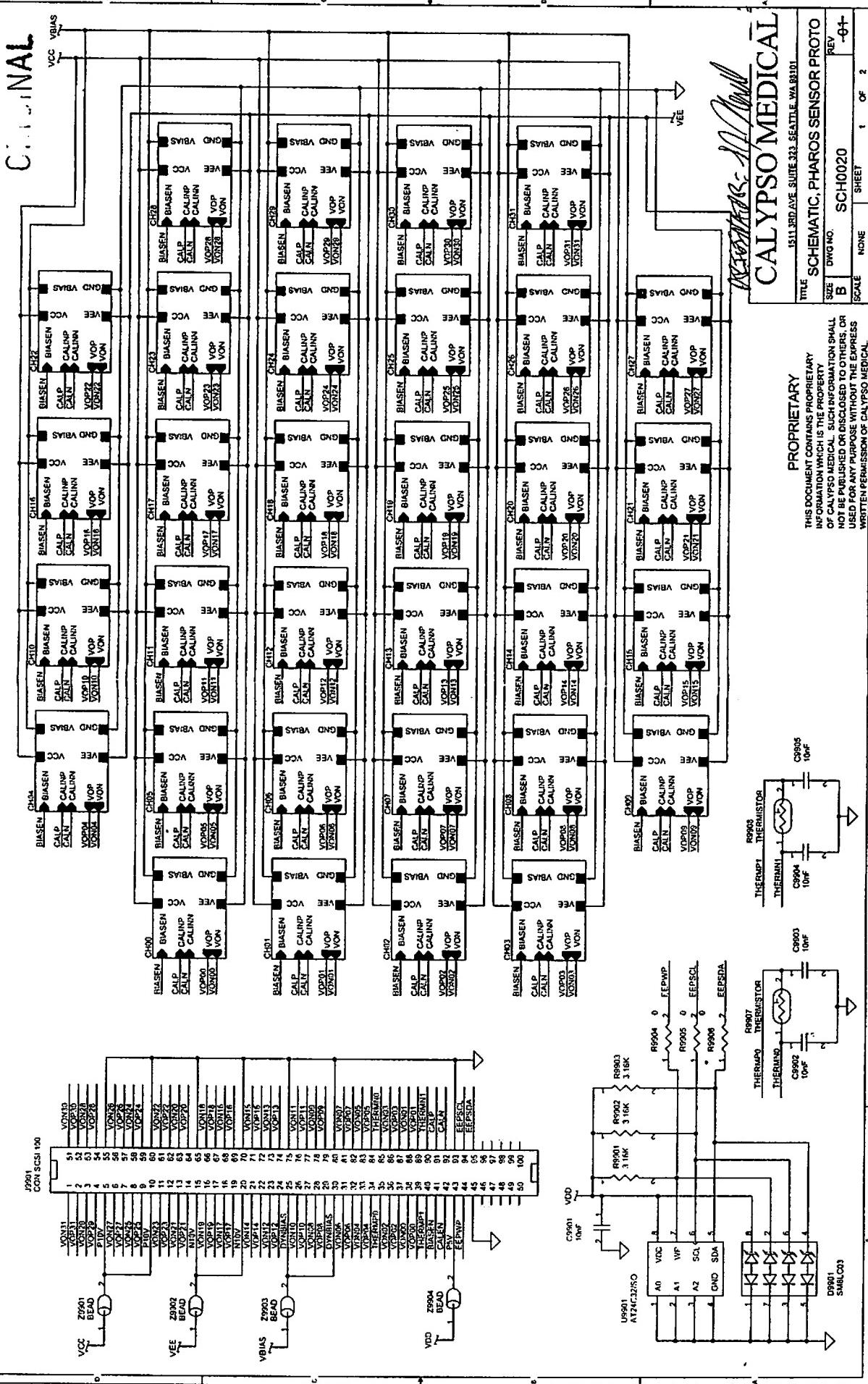
Examiner: Ellsworth Weatherby

AMENDED DECLARATION OF J. NELSON WRIGHT UNDER 37 C.F.R. § 1.131

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

EXHIBIT B

CINNAMAL



REF ID: J901
REV A
DATE: 10/10/01
TITLE: SCHEMATIC, PHAROS SENSOR PROTO

SITE: B
Dwg No.: SCH0020
Rev: -04-
Sheet: 1 OF 2

SCALE: 1:1
X 1
Y 1
Z 1

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